***Full\_Adder***

**DSD:**

**Digital System Design**

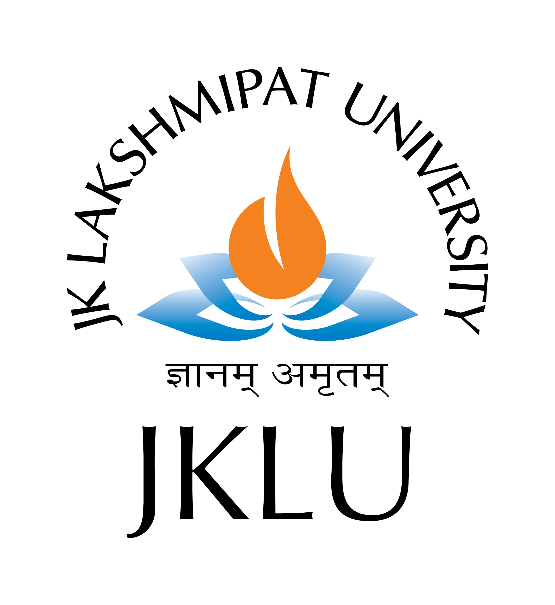
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Design a full adder using tow half adders and OR gate. Use VHDL (Verilog).

module FA\_2(a,b,cin,sum,cout);

input a,b,cin;

output sum,cout;

wire x,y,z;

half\_add h1(.a(a),.b(b),.s(x),.c(y));

half\_add h2(.a(x),.b(cin),.s(sum),.c(z));

or o1(cout,y,z);

endmodule : FA\_2

module half\_add(a,b,s,c);

input a,b;

output s,c;

xor x1(s,a,b);

and a1(c,a,b);

endmodule :half\_add

